

Abstract

A data strobe circuit for prefetching M number of N bit data, N and M being a positive integer, includes a data strobe buffering unit for generating N number of align control signals based on a data strobe signal; a synchronizing block having M number of latch blocks, each for receiving N bit data and outputting the N-1 bit data in a parallel fashion in response to N-1 number of the align control signals and one bit prefetched data in response to the remaining align control signals; and a output block having M number of aligning blocks, each for receiving the N-1 bit data in the parallel fashion, synchronizing the N-1 bit data with the align control signal and outputting the synchronized N-1 bit data as the N-1 bit prefetched data.